REMARKS

Applicant respectfully requests reconsideration and allowance in view of the foregoing amendments and the following remarks. In this response, claims 1 and 6 are amended.

In the Office Action, claims 1-5 stand rejected under 35 U.S.C. §112 as being indefinite for allegedly redefining the term "software direct memory access." Applicant disagrees that the term is defined implicitly or explicitly outside the accepted meaning of the term. Applicant respectfully submits that the distinction proposed by the Office Action is unnecessary because a reasonably skilled artisan will readily comprehend that a reference to software direct memory access is indicative of a direct memory access system or direct memory access process that is implemented in software. Indeed, such a definition is consistent with similar usage of "software" as a qualifier in terms such as "software modem," which term is universally understood in the art to mean a modem that is implemented in software.

Direct memory access (hereinafter "DMA") is well understood in the art as relating to data transfers, as evidenced in the Wikipedia online encyclopedia:

> A DMA transfer essentially copies a block of memory from one device to another. While the CPU initiates the transfer, the transfer itself is performed by the DMA Controller. A typical example is moving a block of memory from external memory to faster, internal (on-chip) memory. Such an operation does not stall the processor, which as a result can be scheduled to perform other tasks. DMA transfers are essential to high performance embedded algorithms.

(See Wikipedia at *http://en.wikipedia.org/wiki/Direct_memory_access*, visited 5/3/2005)

In this definition, the DMA Controller handles a transfer, but there is nothing that supports a requirement to eliminate processor participation. Applicant submits that it is understood in the art that DMA controllers are typically programmable and therefore the DMA controller necessarily includes some processing by a processor.

The Office Action confirms that the term "software DMA" is readily comprehensible. The Office Action asserts that "it is well known that not all devices are hardware DMA compatible, and must be accessed using software DMA" (Page 4, lines 2-3). In the office action, the Examiner exchanged qualifiers to indicate a function implemented in software. Since a software DMA system necessarily requires the use of a processor, a limitation defining software

DMA as requiring "the use of a processor" is unnecessary and unwarranted. Therefore, Applicant respectfully requests withdrawal of the rejection under § 112.

Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,884,027 to Garbus et al. ("Garbus") in view of "Structured Computer Organization" by Tanenbaum.

Regarding Claim 1, the Office Action cites Garbus as teaching first and second processors and a DMA engine and cites Tanenbaum as rendering obvious the feasibility of implementing DMA in software. However, as amended, claim 1 requires a first bus and a second bus, instruction memory coupled to the first and second busses and a processor connected to the first and second busses. The processor executes the software DMA engine and the software DMA engine is capable of transferring data directly between all of a plurality of resources in the system. These limitations, among others, are not taught by Garbus. Tanenbaum merely alleges an ability to make in software that which has been made in hardware and therefore cannot be said to correct the deficiencies of Garbus.

Applicant disagrees with the Office Action's assertion that Garbus anticipates all limitations of the claimed software DMA engine. Garbus is directed to a PCI-PCI bus bridge with an integrated DMA controller. The present invention provides a multiprocessor system in which at least one processor provides DMA capability in software. Thus, not only are the combination and arrangement of components in Garbus significantly different from those of the presently claimed invention, but the apparent objectives of Garbus are inconsistent with the provision of a software DMA engine as taught in the present application.

Nor can it be said that Garbus renders obvious the claimed invention. Prior art DMA systems have been implemented to speed access to memory for a CPU and to extract the CPU from some data transfers from memory to peripherals (see Specification, page 1, lines 6-18). Thus, at the time of the invention, it would appear obvious to a skilled artisan that the implementation of a DMA engine in software would increase – rather than decrease – CPU overhead and would therefore be counterproductive. Therefore, the use of a software DMA engine in a multiprocessor system is counterintuitive, especially when considering a PCI-PCI bridge such as that taught by Garbus.

Therefore, for at these least reasons, Applicant respectfully submits that independent claim 1 is not rendered obvious by the combination of Garbus and Tanenbaum and request withdrawal of the rejection of claim 1.

Regarding claim 6, Applicant has amended claim 6 and submits that Garbus fails to anticipate each and every element of the claim as amended. As discussed above, the Garbus reference does not anticipate or suggest a DMA apparatus implemented in software in a multiprocessor system. Specifically, Garbus is directed to a PCI-PCI bridge and nowhere teaches that one of two or more processors execute software to implement DMA on a computer system. Therefore, Applicants respectfully request withdrawal of claim 6.

Regarding claims 2-5 and claims 7-9, these claims depend from claims 1 and 6, respectively and are patentable for at least the foregoing reasons. In rejecting these claims, the Office Action proposes that certain components in Garbus anticipate or render obvious elements of the present invention. Applicant respectfully disagrees. For example, the Office Action alleges that Garbus teaches data processing as recited in claims 2 and 9 by reference to a listing that includes scatter/gather and unaligned data transfer. Applicant disagrees and notes that claims 2 and 9 recites data filtering, data compacting and data reformatting in addition to data processing. As understood in the art, scatter/gather and unaligned data transfer cannot be said to anticipate or suggest all of the functions recited in these claims. As a specific example, data filtering would not be expected of a data storage method such as scatter/gather or unaligned data transfer. Therefore, for at least these reasons, Applicant submits that Garbus fails to anticipate or render obvious each and every limitation of claims 2-5 and 7-9 and withdrawal of the rejection is respectfully requested.

In summary, for at least the reasons presented above, Garbus combined with Tanenbaum does not teach or suggest a software Direct Memory Access software in a system comprising two or more processors as claimed in the present application. Accordingly, Applicant respectfully submits that claims 1-9 are allowable over the art of record.

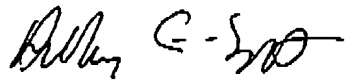
CONCLUSION

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition of allowance and a Notice to that effect is earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 50-2213.

Date: May 4, 2005

Respectfully submitted,



Anthony G. Smyth Reg. No. 55,636
For David H. Jaffer Reg. No. 32,243
Customer No. 27498

PILLSBURY WINTHROP SHAW PITTMAN LLP
2475 Hanover Street
Palo Alto, CA 94304-1114
Tel. No. (650) 233-4510
Fax No. (650) 233-4545
djaffer@pillsburywinthrop.com

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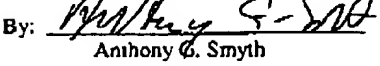
By: 
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